TRIMMING METHOD FOR A TRANSCEIVER USING TWO-POINT MODULATION

5 <u>Cross-Reference to Related Application</u>:

This application is a continuation of copending International

Application No. PCT/DE01/04956, filed December 28, 2001, which

designated the United States and which was not published in

English.

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<u>Background of the Invention</u>:

<u>Field of the Invention</u>:

The invention relates to a trimming method for PLL circuits

which operate on the principle of two-point modulation. The

15 invention relates, in particular, to a method for amplitude

trimming in transceivers for mobile radio systems having a PLL

circuit, which operates on the principle of two-point

modulation, in the transmitter and having a receiver which

operates on the limiter/discriminator principle.

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A low-complexity implementation of a transmitter concept for

transceivers in mobile radio systems is provided by

transmitters having a modulator which operates on the

principle, which is known per se, of two-point modulation, in

25 which it is possible to modulate a PLL (phase locked loop)

circuit with signals whose bandwidth is greater than the PLL

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bandwidth, so that the PLL circuit has a transmission response which is independent of frequency.

Fig. 3 shows, in simplified form, a prior art PLL circuit,
5　which operates on the principle of two-point modulation, for such a transmitter. The circuit has a phase frequency detector (PFD) 1, a charge pump (CP) 2, a loop filter (LF) 3 and a voltage controlled oscillator (VCO) 5 in the forward path. There is provided a frequency divider 6 with divisor N in the
10　feedback path of the modulator.

In order to produce the two-point modulation, analog modulation is introduced into the PLL circuit, which has been stabilized at the channel mid-frequency before the actual
15　transmission process, at a summation point 4 which is located upstream of the voltage controlled oscillator 5 in the forward path and represents a high-pass point (analog modulation which is fed in at this point acts on the output with high-pass filtering provided by the closed control loop), and digital
20　modulation is introduced into the PLL circuit, which has been stabilized at the channel mid-frequency before the actual transmission process, in the feedback path at the frequency divider 6, which represents a low-pass point. The two modulation signals are then superimposed at the output of the
25　PLL circuit so as to produce the desired frequency-independent response.

In this type of transmitter concept, the PLL control loop remains closed. Owing to the requirements for the noise response, the bandwidth of the PLL control loop is furthermore

5 designed to be narrower than would be necessary for transmitting modulated data. Thus, in addition to the pure digital modulation, the analog modulation is used to compensate for the restricted bandwidth in which case, in addition to the analog and digital modulation being

10 synchronized in phase, it is of major importance that the amplitudes of these two modulation signals match.

Owing to the production tolerances in the components that are used for analog modulation, with regard, for example, to the

15 modulation gradient, the production of the modulation voltage and the like, it is necessary to carry out amplitude trimming between the analog modulation and the digital modulation after production. If, furthermore, it is also necessary to take into account influences caused by temperature changes, this

20 amplitude trimming must be carried out before every transmission process.

One prior art trimming method is to introduce the two modulations, to supply the output signal from the PLL circuit

25 to an external measurement receiver, to demodulate it there, and to carry out appropriate amplitude trimming. Since the

voltage controlled oscillator 5 has a non-linear frequency response as a function of the voltage, such amplitude trimming must, however, be carried out for each of a large number of channels, which leads to a long measurement duration and,

5   furthermore, requires that the trimming information be stored in a memory. Furthermore, it is not possible to take account of influences resulting from temperature changes in this way.

A further known trimming method includes the reception and
10   demodulation by the receiver section of the transmitter/receiver. However, a complete second PLL circuit is required in the receiver for this purpose, which, in addition to considerably greater circuit complexity and greater costs associated with this complexity, makes it
15   necessary when using a heterodyne receiver to set this receiver to a frequency which corresponds to the difference between the transmission frequency and the intermediate frequency.

20   The prior art trimming methods thus have the disadvantage that they are associated on the one hand with a long measurement duration and on the other hand with a high level of equipment and circuitry complexity, with correspondingly high costs.

Summary of the Invention:

It is accordingly an object of the invention to provide a trimming method for a transceiver with two-point modulation which overcomes the above-mentioned disadvantages of the

5   heretofore-known devices and methods of this general type and which allows rapid amplitude trimming with little complexity, and which makes it possible to take into account temperature influences.

10 With the foregoing and other objects in view there is provided, in accordance with the invention, a trimming method for a transmitter/receiver having a phase locked loop circuit operating on a two-point modulation principle. The method comprises the following steps:

15 selecting an amplitude of an analog modulation signal based on a modulation shift of a defined digital modulation signal;

applying a predetermined data sequence of the analog modulation signal;

determining a modulation shift of the analog modulation signal
20 at an output of the receiver; and

correcting the amplitude of the analog modulation signal to match a difference between the modulation shift of the digital

modulation signal and the modulation shift of the analog
modulation signal.

In other words, the objects are achieved, according to the

5   invention, with a trimming method for a transmitter/receiver
having a PLL circuit which operates on the principle of two-
point modulation, as follows: selection of the amplitude of an
analog modulation signal on the basis of the modulation shift
of a defined digital modulation signal; application of a

10   predetermined data sequence of the analog modulation signal;
determination of the modulation shift of the analog modulation
signal at an output of the receiver; and correction of the
amplitude of the analog modulation signal to match the
difference between the modulation shift of the digital

15   modulation signal and the determined modulation shift of the
analog modulation signal.

Before carrying out the trimming process, the PLL circuit is
set to a channel mid-frequency before a transmission process,

20   in order to produce a steady state.

The digital modulation signal is preferably deactivated during
the trimming process, in order to prevent the analog
modulation being regulated out when selecting an initial

25   amplitude for the analog modulation signal.

The predetermined data sequence of the analog modulation
signal is furthermore preferably applied to a predetermined
high-pass point in the forward path of the PLL circuit, and
the digital modulation signal is applied to a predetermined
5   low-pass point in the feed-back path of the PLL circuit, thus
resulting in the PLL circuit having an overall transfer
function which is advantageous for the response of the
arrangement.

10   The digital modulation signal is in this case applied in some
suitable manner to a first frequency divider.

If the output signal from the PLL circuit is passed to a
second frequency divider, which is located in a signal path
15   which branches off from the feedback path, is divided in the
second frequency divider and is then supplied as one of the
input signals to the receiver, there is advantageously no need
for a second PLL circuit in the receiver.

20   The divisor of the second frequency divider is in this case
preferably selected such that the output frequency from the
second frequency divider corresponds to the intermediate
frequency of the receiver.

25   Alternatively, an integer value may be selected as the divisor
of the second frequency divider such that the output frequency

from the second frequency divider is essentially close to the intermediate frequency of the receiver, thus resulting in an additional degree of freedom for the selection of the divisor for the second frequency divider, taking into account the

5   actual frequency band of the receiver.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

10   Although the invention is illustrated and described herein as embodied in a trimming method for a transceiver using two-point modulation, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from

15   the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages

20   thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

25   Fig. 1 is a block diagram of a PLL circuit configuration that operates on the principle of two-point modulation and in which

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a trimming method can be used for a transmitter/receiver which uses two-point modulation, based on a preferred exemplary embodiment of the invention;

5   Fig. 2 is a simplified flowchart of the trimming method according to the preferred exemplary embodiment of the invention; and

Fig. 3 is a simplified block diagram of a prior art PLL
10   circuit that operates on the principle of two-point modulation.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and
15   first, particularly, to Fig. 1 thereof, there is shown a PLL (phase locked loop) circuit configuration which operates on the principle of two-point modulation and in which a trimming method (tuning, calibrating) can be used for a transmitter/receiver (transceiver) using two-point modulation,
20   according to the invention.

Similarly to the prior art PLL circuit shown in Fig. 3, there is provided a phase frequency detector (PFD) 1, a charge pump (CP) 2, a loop filter (LF) 3, a summation point 4 and a
25   voltage controlled oscillator (VCO) 5 in the forward path, i.e., in the signal flow direction. There is also provided a

first frequency divider 6 with a first divisor N_1 in the feedback path, of the PLL circuit configuration according to the invention. Also, the PLL circuit is likewise already stabilized at the channel mid-frequency before the
5   transmission process.

There is provided, in accordance with the invention, a second frequency divider 7 with a second divisor N_2 in a signal path that branches off from the feedback path of the PLL circuit
10   after the first frequency divider 6. The second frequency divider 7 is followed by an FM demodulator 8 as part of a heterodyne receiver (which is not illustrated) which is known per se and operates on the limiter/discriminator principle.

15   The method of operation of the circuit configuration illustrated in Fig. 1 will be described in more detail in the following text.

First of all, a reference frequency f_R is supplied to a first
20   input of the phase frequency detector 1 in the PLL circuit. The reference frequency f_R is compared in the phase frequency detector 1 with the frequency in the feedback path downstream from the first frequency divider 6, and a control signal is produced, which is processed in a known manner in the charge
25   pump 2, the loop filter 3 and the voltage controlled oscillator 5. An output signal at the frequency f_{vco} thus

appears at the output of the voltage controlled oscillator.
The output signal f_{vco} in the voltage controlled oscillator 5
is supplied to the first frequency divider 6, which is located
in the feedback path of the PLL circuit and whose divisor is N_1

5   and the output of this first frequency divider 6 in
consequence produces a signal at the frequency f_{vco}/N_1.

In order to produce the two-point modulation, analog
modulation is introduced into the PLL circuit at the summation

10   point 4 which is located upstream of the voltage controlled
oscillator 5 in the forward path of the PLL circuit, and
digital modulation is introduced into the PLL circuit at the
first frequency divider 6 in the feedback path of the PLL
circuit.

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The digitally modulated output signal f_{vco}/N_1 from the first
frequency divider 6 is then supplied to a second input of the
phase frequency detector 1 and to a second frequency divider
7, which is located in a signal path which branches off from

20   the feedback path of the PLL circuit after the first frequency
divider 6 and whose divisor is N_2.

The second frequency divider 7 divides the output signal f_{vco}/N_1
from the first frequency divider 6 by its divisor N_2, so that

25   the output of the second frequency divider 7 produces a
further divided output signal at the frequency $f_{vco}/(N_2*N_1)$.

The output signal $f_{vco}/(N_2*N_1)$ from the second frequency divider 7 is then supplied to the downstream FM demodulator 8, and is demodulated by it.

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The divisor N_2 of the second frequency divider 7 is in this case preferably selected such that the output frequency $f_{vco}/(N_2*N_1)$ corresponds to the intermediate frequency of the heterodyne receiver. This means that, advantageously, there is

10   no need for a second complete PLL control loop in the receiver for down-mixing the output signal f_{vco} from the voltage controlled oscillator 5.

Since, owing to the possible frequency offsets, the receiver

15   is generally suitable for a wider frequency range, the divisor N_2 for the second frequency divider 7 may also alternatively be selected such that its output frequency $f_{vco}/(N_2*N_1)$ is located essentially in the vicinity of the intermediate frequency, corresponding to a frequency offset. The precise location of

20   the output frequency $f_{vco}/(N_2*N_1)$ is, however, known and can thus be taken into account in an appropriate manner.

This advantageously results in an additional degree of freedom for the selection of the divisor N_2, as will be explained in

25   more detail in the following text.

The output signal from the frequency divider 7 is, furthermore, a digital signal. Since the downstream receiver operates on the limiter/discriminator principle and can also be designed to process the discrete-value, continuous output

5   signals from the limiter in both a digital manner and in analog manner, the digital output signal from the frequency divider 7 is in consequence suitable for use as an input signal for this receiver, if it is fed in after the limiter.

10.   It should be noted that two output signals, phase-shifted through 90°, are required from the second frequency divider 7 when processing complex-value signals, in an equivalent manner to the complex-value limiter output signals.

15   A refinement such as this is feasible in particular for even-numbered divisors N_2, which can advantageously be selected on the basis of the additional degree of freedom as mentioned above.

20   The trimming method which can be used for the PLL circuit as described above will be described in more detail in the following text with reference to the flowchart shown in Fig. 2.

25   In a first step S1, the PLL circuit is as a preparatory measure set to the channel mid-frequency before a transmission

process. A setting process such as this is required in any case for operation, even if the trimming method is not carried out.

5   Analog modulation and digital modulation are then applied, as described above, in a second step S2.

In a third step S3, the digital modulation introduced at the first frequency divider 6 is deactivated, and the amplitude of

10   the analog modulation signal which is introduced at the summation point 4 is selected such that it corresponds to the modulation shift which is set for the digital modulation signal and which has no tolerances by virtue of its digital form.

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The digital modulation is thus deactivated during the trimming process, and only the analog modulation is used. Since the closed PLL control loop would regulate out the analog modulation, the assessment of the influence of this modulation

20   must be carried out at times defined in advance during the transient phase.

A suitable data sequence of the analog modulation is then applied in a fourth step S4.

25

The modulation shift produced by the analog modulation is then determined at the output of the demodulator 8 of the receiver, in a fifth step S5.

5   After this, the difference between the modulation shift of the nominally set digital modulation signal and the determined modulation shift of the applied analog modulation signal is determined in a sixth step S6.

10   Finally, in a seventh step S7, the amplitude of the applied analog modulation signal is corrected in order to match the difference between the nominally set digital modulation shift and the determined analog modulation shift.

15   The described method thus makes it possible to obtain qualitative statements relating to the error that has occurred in a simple manner, and to determine a suitable correction value simply by subtraction.

20   As has been described above, in a method for amplitude trimming in transceivers for mobile radio systems having a PLL circuit, which operates on the principle of two-point modulation, in the transmitter and having a receiver which operates on the limiter/discriminator principle, the amplitude
25   of an analog modulation signal is selected on the basis of a modulation shift of a defined digital modulation signal, a

predetermined data sequence of the analog modulation signal is applied, the modulation shift of the analog modulation signal at the output of a demodulator of the receiver is determined, and the amplitude of the analog modulation signal is corrected

5 in order to match the difference between the modulation shift of the digital modulation signal and the determined modulation shift of the analog modulation signal.